## CLAIMS

WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

a watchdog timer coupled to receive a reset input upon a predetermined change in a system state, wherein the watchdog timer is further configured to provide an indication in response to an expiration of the watchdog timer; and

logic configured to receive a request for a system reset, wherein the logic is configured to query the watchdog timer for the expiration of the watchdog timer in response to receiving the request for the system reset.

2. The integrated circuit of claim 1, wherein the logic comprises a microcontroller configured as an Alert Standard Format management engine, wherein the microcontroller is further configured to receive Alert Standard Format sensor data over a first external bus.

3. The integrated circuit of claim 2, further comprising:

a second bus interface logic for coupling to a first internal bus, wherein data from the first external bus is routable by the embedded Alert Standard Format management engine over the first internal bus.

4. The integrated circuit of claim 1, wherein the logic comprises an RMCP unit configured to receive RMCP commands from an external management server.

5. The integrated circuit of claim 1, further comprising:

an embedded Ethernet controller coupled to a first internal bus.

6. The integrated circuit of claim 5, wherein the embedded Ethernet controller is configured to route the RMCP commands from the external management server to the RMCP unit.

7. The integrated circuit of claim 1, further comprising:

a first bus interface logic for coupling to the first external bus.

8. The integrated circuit of claim 7, wherein the integrated circuit comprises a bridge, wherein the bridge further comprises:

a third bus interface logic for coupling to a second external bus.

9. The integrated circuit of claim 8, wherein the bridge comprises a south bridge, wherein the first external bus is configurable as a first input/output bus.

10. The integrated circuit of claim 9, wherein the first input/output bus is an SMBus.

11. The integrated circuit of claim 1, wherein the reset input is provided to the watchdog timer by the microcontroller.

12. The integrated circuit of claim 1, wherein the reset input is provided to the watchdog timer from an external processor.

13. The integrated circuit of claim 1, further comprising:

a register configure to store system status information.

14. The integrated circuit of claim 13, wherein the microcontroller is further configured to read the system status information from the register in response to the indication.

15 The integrated circuit of claim 14 wherein the microcontroller is further configured to provide the system status information to an external management server.

16. An integrated circuit, comprising:

a timing means coupled to receive a reset input upon a predetermined change in a system state, wherein the timing means is further configured to provide an indication in response to an expiration of the timing means; and

logic means configured to receive a request for a system reset, wherein the logic means is configured to query the timing means for the expiration of the timing means in response to receiving the request for the system reset.

17. The integrated circuit of claim 16, wherein the logic means is further configured as an Alert Standard Format management engine, wherein the logic means is further configured to receive Alert Standard Format sensor data over a first external communications means.

18. The integrated circuit of claim 17, further comprising:

a first internal communications means; and

a second interface means for coupling to the first internal communications means, wherein data from the first external communications means is routable by the logic means over the first internal communications means.

19. The integrated circuit of claim 16, wherein the logic means is configured to receive RMCP commands from an external management means.

20. The integrated circuit of claim 16, further comprising:

an embedded networking means coupled to the first internal communications means.

21. The integrated circuit of claim 20, wherein the embedded networking means is configured to route the RMCP commands from the external management means to the logic means.

22. The integrated circuit of claim 16, further comprising:

a first interface means for coupling to a first external communications means;

23. The integrated circuit of claim 22, wherein the integrated circuit comprises a bridge, wherein the bridge further comprises:

a third interface means for coupling to a second external communications means.

24. The integrated circuit of claim 23, wherein the bridge comprises a south bridge, wherein the first external communications means is configurable as a first input/output bus.

25. The integrated circuit of claim 16, wherein the reset input is provided to the timing means by the logic means.

26. The integrated circuit of claim 16, wherein the reset input is provided to the timing means from an external processing means.

27. The integrated circuit of claim 16, further comprising:

a storage means configure to store system status information.

28. The integrated circuit of claim 27, wherein the logic means is further configured to read the system status information from the storage means in response to the indication.

29. The integrated circuit of claim 27, wherein the logic means is further configured to provide the system status information to an external management means.

30. A computer system, comprising:

a first external bus; and

an integrated circuit, the integrated circuit comprising:

a first bus interface logic for coupling to the first external bus;

a watchdog timer coupled to receive a reset input upon a predetermined change in a system state, wherein the watchdog timer is further configured to provide an indication in response to an expiration of the watchdog timer; and

logic configured to receive a request for a system reset, wherein the logic is configured to query the watchdog timer for the expiration of the watchdog timer in response to receiving the request for the system reset.

31. The computer system of claim 30, wherein the logic comprises a microcontroller configured as an Alert Standard Format management engine, wherein the microcontroller is further configured to receive Alert Standard Format sensor data over the first external bus.

32. The computer system of claim 31, with the integrated circuit further comprising:

a second bus interface logic for coupling to a first internal bus, wherein data from the first external bus is routable by the embedded Alert Standard Format management engine over the first internal bus.

33. The computer system of claim 30, wherein the logic comprises an RMCP unit configured to receive RMCP commands from an external management server.

34. The computer system of claim 33, with the integrated circuit further comprising:

an embedded Ethernet controller coupled to the first internal bus.

35. The computer system of claim 34, wherein the embedded Ethernet controller is configured to route the RMCP commands from the external management server to the RMCP unit.

36. The computer system of claim 30, further comprising:

a second external bus; and

wherein the integrated circuit comprises a bridge, wherein the bridge further comprises:

a third bus interface logic for coupling to the second external bus.

37. The computer system of claim 36, wherein the bridge comprises a south bridge, and wherein the first external bus is configurable as a first input/output bus.

38. The computer system of claim 37, wherein the first input/output bus is an SMBus.

39. The computer system of claim 30, wherein the reset input is provided to the watchdog timer by the logic.

40. The computer system of claim 30, further comprising:

a processor configured to provide the reset input to the watchdog timer.

41. The computer system of claim 30, with the integrated circuit further comprising:

a register configured to store system status information.

42. The computer system of claim 41, wherein the logic is further configured to read the system status information from the register in response to the indication.

43. The computer system of claim 41, wherein the logic is further configured to provide the system status information to an external management server.

44. A computer system, comprising:

a first external communications means; and

an integrated circuit, the integrated circuit comprising:

a first interface means for coupling to the first external communications means;

a timing means coupled to receive a reset input upon a predetermined change in a system state, wherein the timing means is further configured to provide an indication in response to an expiration of the timing means; and

logic means configured to receive a request for a system reset, wherein the logic means is configured to query the timing means for the expiration of the timing means in response to receiving the request for the system reset.

45. The computer system of claim 44, wherein the logic means is configured as an Alert Standard Format management engine, wherein the logic means is further configured to receive Alert Standard Format sensor data over the first external communications means.

46. The computer system of claim 44, wherein the logic means is further configured to receive RMCP commands from an external management means.

47. The computer system of claim 44, with the integrated circuit further comprising:

a first internal communications means; and

an embedded networking means coupled to the first internal communications means.

48. The computer system of claim 47, wherein the embedded networking means is configured to route the RMCP commands from the external management means to the logic means.

49. The computer system of claim 44, wherein the reset input is provided to the timing means by the logic means.

50. The computer system of claim 44, further comprising:

a processing means configured to provide the reset input to the timing means.

51. The computer system of claim 44, with the integrated circuit further comprising:

a storage means configured to store system status information.

52. The computer system of claim 51, wherein the logic means is further configured to read the system status information from the storage means in response to the indication.

53. The computer system of claim 51, wherein the logic means is further configured to provide the system status information to an external management means.

54. A method of operating a computer system, the method comprising:

receiving a request for a system state change;

checking for status of a watchdog timer;

denying the request for the system state change if the watchdog timer has not expired; and

performing the request for the system state change if the watchdog timer has expired.

55. The method of claim 54, further comprising:

resetting the watchdog timer in response to a change in system state.

56. The method of claim 54, wherein receiving the request for the system state change comprises receiving the request for a system reset, a system reboot, or a system boot.

57. The method of claim 54, wherein receiving the request for the system state change comprises receiving an RMCP request for the system state change.

58. The method of claim 54, further comprising:

checking a storage location for an entry indicative of a first condition;

wherein checking for status of the watchdog timer comprises checking for status of the watchdog timer if the entry is indicative of the first condition;

wherein denying the request for the system state change if the watchdog timer has not expired comprises denying the request for the system state change if the entry is indicative of the first condition and the watchdog timer has not expired;

wherein performing the request for the system state change if the watchdog timer has expired comprises performing the request for the system state change if the entry is indicative of the first condition and the watchdog timer has expired;

and the method further comprising:

performing the request for the system state change if the entry is indicative of a second condition.

59. A method of operating a computer system, the method comprising the steps of:

receiving a request for a system state change;

checking for status of a watchdog timer;

denying the request for the system state change if the watchdog timer has not expired; and

performing the request for the system state change if the watchdog timer has expired.

60. The method of claim 59, further comprising the step of:

resetting the watchdog timer in response to a change in system state.

61. The method of claim 59, wherein the step of receiving the request for the system state change comprises the step of receiving the request for a system reset, a system reboot, or a system boot.

62. The method of claim 59, wherein the step of receiving the request for the system state change comprises the step of receiving an RMCP request for the system state change.

63. The method of claim 59, further comprising the step of:

checking a storage location for an entry indicative of a first condition;

wherein the step of checking for status of the watchdog timer comprises the step of checking for status of the watchdog timer if the entry is indicative of the first condition;

wherein the step of denying the request for the system state change if the watchdog timer has not expired comprises the step of denying the request for the system state change if the entry is indicative of the first condition and the watchdog timer has not expired;

wherein the step of performing the request for the system state change if the watchdog timer has expired comprises the step of performing the request for the system state change if the entry is indicative of the first condition and the watchdog timer has expired;

and the method further comprising the step of:

performing the request for the system state change if the entry is indicative of a second condition.

64. A computer readable medium encoded with instructions that, when executed by a computer system, performs a method for operating the client computer system, the method comprising:

receiving a request for a system state change;

checking for status of a watchdog timer;

denying the request for the system state change if the watchdog timer has not expired; and

performing the request for the system state change if the watchdog timer has expired.

65. The computer readable medium of claim 64, with the method further comprising:

resetting the watchdog timer in response to a change in system state.

66. The computer readable medium of claim 64, wherein receiving the request for the system state change comprises receiving the request for a system reset, a system reboot, or a system boot.

67. The computer readable medium of claim 64, wherein receiving the request for the system state change comprises receiving an RMCP request for the system state change.

68. The computer readable medium of claim 64, the method further comprising:

checking a storage location for an entry indicative of a first condition;

wherein checking for status of the watchdog timer comprises checking for status of the watchdog timer if the entry is indicative of the first condition;

wherein denying the request for the system state change if the watchdog timer has not expired comprises denying the request for the system state change if the entry is indicative of the first condition and the watchdog timer has not expired;

wherein performing the request for the system state change if the watchdog timer has expired comprises performing the request for the system state change if the entry is indicative of the first condition and the watchdog timer has expired;

and the method further comprising:

performing the request for the system state change if the entry is indicative of a second condition.